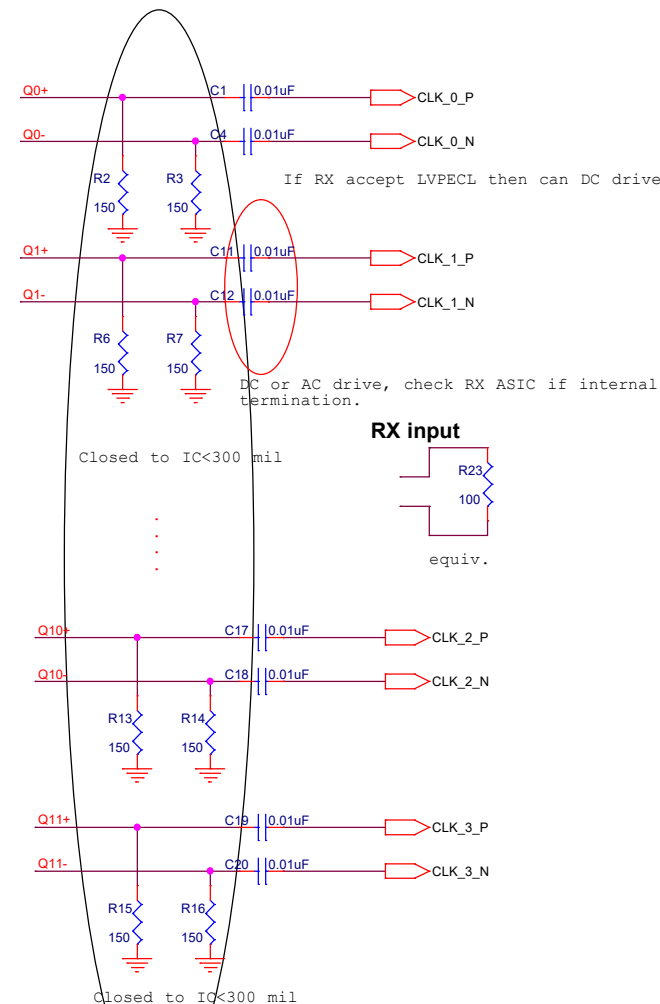
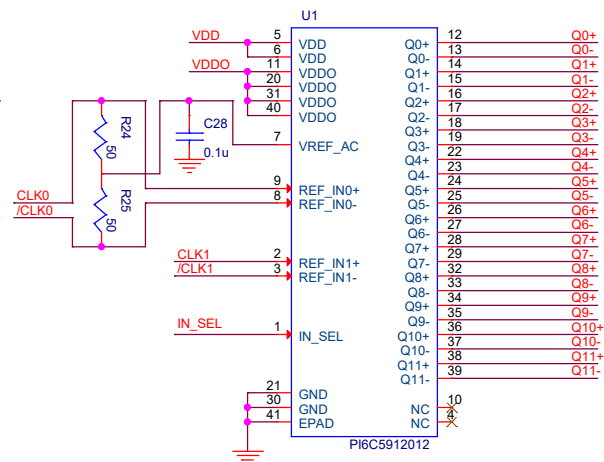


**IN\_SEL:**  
Set IN\_SEL logic in R8/JP1  
0: REF\_IN0 is input  
1: REF\_IN1 is input (default)



### App Note:

1. Select REF\_IN0 or REF\_IN1 as input ;
- 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO...etc)
- 2.2 VDD uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Place 150ohm pull-down in comp. side close to pin <=300mil.
4. To drive RX quiv. 100ohm diff. load, check if chipset has internal termination.
5. When in AC input drive, VREF\_AC is used.
6. If use CMOS XO drive, needs 1k pull-up/down at REF\_IN\_pin, refer to datasheet app. page
7. Connect epad >= 8 vias to GND plane

Title		
PI6C5912012 Application Schematic		
Size B	Document Number Diodes Inc. Clock IC Application Engineering	Rev 1.0
Date: Tuesday, November 26, 2024	Sheet 1	of 1